**MIDTERM EXAMINATION**
**CS501- Advance Computer Architecture**

**Question No: 1 ( Marks: 1 ) - Please choose one**
For any of the instructions that are a part of the instruction set of the SRC, there are cerain_____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
►Register
**►Control signals (Page 171)**
►Memory
►None of the given

**Question No: 2 ( Marks: 1 ) - Please choose one**
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.
►8-bits
►16-bits
**►32-bits (Page 157)**
►64-bits

**Question No: 3 ( Marks: 1 ) - Please choose one**
What is the instruction length of the FALCON-A processor?
►8-bits
**►16-bits (Page 134)**
►32-bits
►64-bits

**Question No: 4 ( Marks: 1 ) - Please choose one**
_____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus.
**►LPC (Page 172)**
►INC4
►LC
►I

**Question No: 5 ( Marks: 1 ) - Please choose one**
Which one of the following is a bi-stable device, capable of storing one bit of information?
►Decoder
►**Flip-Flop (Page 76)**
►Multiplexer
►Diplexer

**Question No: 6 ( Marks: 1 ) - Please choose one**
Which instruction is used to store register to memory using relative address?
►ld instruction
►ldr instruction
►lar instruction
►**str instruction (Page 48)**

**Question No: 7 ( Marks: 1 ) - Please choose one**
Which field of the machine language instruction is the "type of operation" that is to be performed?
►**Op-code (Page 33)**
►CPU registers
►Momory cells
►I/O locations

**Question No: 8 ( Marks: 1 ) - Please choose one**
The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]
►Add R3, 56
►lar R3, 56
►**ldr R3, 56 (Page 56)**
►str R3, 56

**Question No: 9 ( Marks: 1 ) - Please choose one**
_____ operation is required to change the processor's state to a known, defined value.
►Change
►**Reset (Page 194)**
►Update
►None of the given

**Question No: 10 ( Marks: 1 ) - Please choose one**
which type of instructions help in changing the flow of the program as and when required?
►Arithmetic
►**Control (Page 137)**
►Data transfer
►Floating point

**Question No: 11 ( Marks: 1 ) - Please choose one**
Which one of the following registers holds the address of the next instruction to be executed?
►Accumulator
►Address Mask
►Instruction Register
**►Program Counter (Page 151)**

**Question No: 12 ( Marks: 1 ) - Please choose one**
Which one of the following is the memory organization of EAGLE processor?
**►8-bits (Page 112)**
►16-bits
►32-bit
►64-bits

**Question No: 13 ( Marks: 1 ) - Please choose one**
The external interface of FALCON-A consists of a _____address bus and _____a data bus.
►8-bit. 8-bit
**►16-bit. 16-bit** Click here for detail
►16-bit. 24-bit
►16-bit. 32-bit

**Question No: 14 ( Marks: 1 ) - Please choose one**
Type A of SRC has which of the following instructions?
A) andi, instruction
b) No operation or nop instruction
c) lar instruction
d) ldr instruction
e) Stop operation or stop instruction
►& (b)
►(b) & (c)
►& (e)
**►(b) & (e) (Page 47)**

**MIDTERM EXAMINATION**
**CS501- Advance Computer Architecture**

**Question No: 1 ( Marks: 1 ) - Please choose one**
**What is the instruction length of the SRC processor?**

► 8 bits
► 16 bits
► **32 bits (Page 134)**
► 64 bits

**Question No: 2 ( Marks: 1 ) - Please choose one**
Which one of the following is the memory organization of **FALCON-E processor?**

► $2^8$ * 8 bits
► $2^{16}$ * 8 bits
► **$2^{32}$ * 8 bits (Page 124)**
► $2^{64}$ * 8 bits

**Question No: 3 ( Marks: 1 ) - Please choose one**
**"If P = 1, then load the contents of register R1 into register R2".**
**This statement can be written in RTL as:**

► R1 ¬ R2
► P: R1 ¬ R2
► **P: R2 ¬ R1 (not confirms) click here for detail**
► P: R2 ¬ R1, P: R1 ¬ R2

**Question No: 4 ( Marks: 1 ) - Please choose one**
The instruction ----------will **load** the register R3 with the contents of the memory location M [PC+56]
► Add R3, 56
► lar R3, 56
► **ldr R3, 56 (Page 47) rep**
► str R3, 56

**Question No: 5 ( Marks: 1 ) - Please choose one**
----------are faster than cache memory
► Accumulator register
► **CPU registers (Page 33)**
► I/O devices
► ROM

**Question No: 6 ( Marks: 1 ) - Please choose one**
**P: R3 ¬ R5**
**MAR ¬ IR**
These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

- ► Arrow ¬
- ► Colon :
- ► **Comma , (Page 69)**
- ► Parentheses ()

**Question No: 7 ( Marks: 1 ) - Please choose one**
Prefetching can be considered a primitive form of----------
► **Pipelining (Page 42)**
► Multi-processing
► Self-execution
► Exception

**Question No: 8 ( Marks: 1 ) - Please choose one**
The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------
► **Exception** **Click here for detail**
► Function
► Stack
► Thread

**Question No: 9 ( Marks: 1 ) - Please choose one**
Which one of the following circuit design levels is called the gate level?
► **Logic Design Level (Page 22)**
► Circuit Level
► Mask Level
► None of the given

**Question No: 10 ( Marks: 1 ) - Please choose one**
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.

- ► **LPC (Page 172) rep**
- ► INC4
- ► LC
- ► Cout

**Question No: 11 ( Marks: 1 ) - Please choose one**
_____ operation is required to change the processor's state to a known, defined value.

- ► Change
- ► **Reset (Page 194) rep**
- ► Update
- ► None of the given

**Question No: 12 ( Marks: 1 ) - Please choose one**
There are _____ types of reset operations in SRC

- ► **Two (Page 195)**
- ► Three
- ► Four
- ► Five

**Question No: 13 ( Marks: 1 ) - Please choose one**
_____ controller controls the sequence of the flow of microinstructions.

- ► Multiplexer
- ► **Microprogram (Page 225)**
- ► ALU
- ► None of the given

**Question No: 14 ( Marks: 1 ) - Please choose one**
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

- ► 8-bits
- ► 24-bits
- ► **32-bits (Page 157) REP**
- ► 64-bits

**Question No: 15 ( Marks: 1 ) - Please choose one**
**Which of the following statement(s) is/are correct about Reduced Instruction Set Computer (RISC) architectures.**

(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) A comparatively large number of user registers are available.
(iv) Instructions can be easily decoded through hard-wired control units.

- ► (i) and (iii) only
- ► (i), (iii) and (iv)
- ► (i), (ii) and (iii) only
- ► (i),(ii),(iii) and (iv)

**Question No: 16 ( Marks: 1 ) - Please choose one**
Which one of the following register holds the instruction that is being executed?

- ► Accumulator
- ► Address Mask
- ► **Instruction Register (Page 152)**
- ► Program Counter

## CS501-Advance Computer Architecture Midterm

**Question No: 1 ( Marks: 1 ) - Please choose one**
_____all memory systems are dumb, in that they respond to only two commands: read or write
**Virtually Computer Systems Design And Architecture, 2/E**
Logically
Physically
None of These

**Question No: 2 ( Marks: 1 ) - Please choose one**
To access an operand in memory, the CPU must first generate an address, which it then issues to the _____
**MEMORY Computer Systems Design And Architecture, 2/E**
REGISTER
DATA BUS
ALL OF ABOVE

**Question No: 3 ( Marks: 1 ) - Please choose one**
_____ or Branch instructions affect the order in which instructions are performed, or control the flow of the program
**Control Computer Systems Design And Architecture, 2/E**
DATA MOVMENT
Arithmetic
LOGICAL

**MIDTERM EXAMINATION**
**CS501 - ADVANCE COMPUTER ARCHITECTURE**

**Question No: 1 ( Marks: 1 ) - Please choose one**
The code size of 2-address instruction is _____.
► 5 bytes
► **7 bytes (Page 36)**
► 3 bytes
► 2 bytes

**Question No: 2 ( Marks: 1 )- Please choose one**
The data movement instructions _____ data within the machine and to or from input/output devices.
► Store
► Load
► **Move** Click here for detail
► None of Above

**Question No: 3 ( Marks: 1 ) - Please choose one**
Register-register instructions use _____ memory operands out of a total of 3 operands
► 1
► 3
► **0 (Page 37)**
► 2

**Question No: 4 ( Marks: 1 ) - Please choose one**
_____all memory systems are dumb, in that they respond to only two commands: read or write.
► **Virtually Computer Systems Design And Architecture, 2/E Rep**
► Logically
► Physically
► None of Above

**Question No: 5 ( Marks: 1 ) - Please choose one**
Flip-flop is a _____device, capable of storing one bit of Information
► **Bi-stable (Page 76)**
► Unit-stable
► Stable
► Storage

## CS501 Advance Computer Architecture
## Quiz No.1

**Question # 1 of 10 ( Marks: 1 ) - Please choose one**
In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?

- ►**Direct Addressing Mode** **Click here for detail**
- ►Immediate addressing mode
- ►Indirect Addressing Mode
- ►Register (Direct) Addressing Mode

**Question # 2 of 10 ( Marks: 1 ) - Please choose one**
Execution time of a program with respect to the processor is calculated as:

- ►Execution Time = IC x CPI x MIPS
- ►**Execution Time = IC x CPI x T (Page 254)**
- ►Execution Time = CPI x T x MFLOPS
- ►Execution Time = IC x T

**Question # 3 of 10 ( Marks: 1 ) - Please choose one**
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------

- ►compiler
- ►**cross assembler (Page 26)**
- ►debugger
- ►linker

**Question # 4 of 10 ( Marks: 1 ) - Please choose one**
What functionality is performed by the instruction "lar R3, 36" of SRC?

- ►It will load the register R3 with the contents of the memory location M [PC+36]
- ►**It will load the register R3 with the relative address itself (PC+36). (Page 48)**
- ►It will store the register R3 contents to the memory location M [PC+36]
- ►No operation

**Question # 5 of 10 ( Marks: 1 ) - Please choose one**
Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
Select correct option:

- ►**:= (Page 66)**
- ►&
- ►%
- ►©

**Question # 6 of 10 ( Marks: 1 ) - Please choose one**
What is the working of Processor Status Word (PSW)?

►**To hold the current status of the processor. (Page 28)**
►To hold the address of the current process
►To hold the instruction that the computer is currently processing
►To hold the address of the next instruction in memory that is to be executed

**Question # 7 of 10 ( Marks: 1 ) - Please choose one**
Almost every commercial computer has its own particular ---------- language
►3GL
►English language
►Higher level language
►**assembly language (Page 25)**

**Question # 8 of 10 ( Marks: 1 ) - Please choose one**
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?

►Arithmetic/logic
►**Load/store (Page 141)**
►Test/branch
►None of the given

**Question # 9 of 10 ( Marks: 1 ) - Please choose one**
What functionality is performed by the instruction "str R8, 34" of SRC?

►It will load the register R8 with the contents of the memory location M [PC+34]
►It will load the register R8 with the relative address itself (PC+34).
►**It will store the register R8 contents to the memory location M [PC+34] (Page 48)**
►No operation

**Question # 10 of 10 ( Marks: 1 ) - Please choose one**
What does the instruction "ldr R3, 58" of SRC do?

►**It will load the register R3 with the contents of the memory location M [PC+58] (Page 47)**
►It will load the register R3 with the relative address itself (PC+58).
►It will store the register R3 contents to the memory location M [PC+58]
►No operation

## CS501- Advance Computer Architecture
## Quiz No.1

**Question # 1 of 10 ( Marks: 1 ) - Please choose one**
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

►**Processor-Memory-Switch level (PMS level)** **(Page 22)**
►Instruction Set Level
►Register Transfer Level
►None of the given

**Question # 2 of 10 ( Marks: 1 ) - Please choose one**
Which of the instruction is used to load register from memory using a relative address?

►ld instruction
►**ldr instruction** **(Page 47)**
►lar instruction
►str instruction

**Question # 3 of 10 ( Marks: 1 ) - Please choose one**
For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory
►Jump
►Control
►**load/store** **(Page 89)**
►None of the given

**Question # 4 of 10 ( Marks: 1 ) - Please choose one**
The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
►Jump and branch format instructions
►Immediate format instructions
►**Register format instructions** **Click here for detail**

## CS501 Advance Computer Architecture
## Quiz No.2

**Question # 1 of 10 (Marks: 1) - Please choose one**
What is the size of the memory space that is available to FALCON-A processor?
►2^8 bytes
**►2^16 bytes (Page 90)**
►2^32 bytes
►2^64 bytes

**Question # 2 of 10 (Marks: 1) - Please choose one**
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
►IR<16..0>
**►IR<15..0> (Page 105)**
►IR<16..1>
►IR<15..1>

**Question # 3 of 10 (Marks: 1) - Please choose one**
Which one of the following portions of an instruction represents the operation to be performed?
►Address
►Instruction code
►Opcode
**►Operand (Page 134)**

**Question # 4 of 10 (Marks: 1) - Please choose one**
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3

►Opcode= R1, DR=ADD, SA=R2, SB=R3
**►Opcode= ADD, DR=R1, SA=R2, SB=R3 (Page 34)**
►Opcode= R2, DR=ADD, SA=R1, SB=R3
►Opcode= ADD, DR=R3, SA=R2, SB=R1

**Question # 5 of 10 (Marks: 1) - Please choose one**
What does the word 'D' in the 'D-flip-Flop' stands for?

**►Data** Click here for detail
►Digital
►Dynamic
►Double

**Question # 6 of 10 (Marks: 1) - Please choose one**
Which one of the following is the code size and the Number of memory bytes respectively for a 2-address instruction?
►4 bytes, 7 bytes
►7 bytes, 16 bytes (Page 36)
►10 bytes, 19 bytes
►13 bytes, 22 bytes

Question # 7 of 10 (Marks: 1) - Please choose one
Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?
►Base address
►Binary address
►Effective address **Click here for detail**
►All of the given

**Question # 8 of 10 (Marks: 1) - Please choose one**
Whic of the following statements is/are true about RISC processors' claimed advantages over CISC processors? (a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution. (b) RISC CPUs outperform CISC CPU's in procedural programming environments. (c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction. (d) It is easier to maintain the "family concept" in RISC CPUs.

► (a), (b) &(c)
► (b), (c) & (e)
► (c), (d) & (e)
► **(a), (c) & (d)**

**Question # 9 of 10 (Marks: 1) - Please choose one**
Which one of the following is/are the features of Register Transfer Language?
a) It is a symbolic language
b) It is describing the internal organization of digital computers
c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers
d) It is high level language

► **(b) only**
► **(a) & (b) only** Click here for detail
► (a) ,(b) & (d)
► (b),(c) & (d)

**Question # 10 of 10 (Marks: 1) - Please choose one**
Motorola MC68000 is an example of ---------microprocessor.

►**CISC (Page 148)**
►RISC
►SRC
►FALCON

**Question # 1 of 10 (Marks: 1) - Please choose one**
Which one of the following registers holds the instruction that is being executed?
►Accumulator
►Address Mask
►**Instruction Register (Page 152) rep**
►Program Counter

**Question # 2 of 10 (Marks: 1) - Please choose one**
The external interface of FALCON-A consists of a _____ data bus.
►8-bit
►**16-bit (Page 167)**
►24-bit
►32-bit

**Question # 3 of 10 (Marks: 1) - Please choose one**
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:

►**Perfecting** **Click here for detail**
►Pipelining
►Superscalar operation
►Speedup

**Question # 4 of 10 (Marks: 1) - Please choose one**
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:

►Backward compatibility
►Data migration
►Reverse engineering
►**Upward compatibility** click here for def

**Question # 5 of 10 (Marks: 1) - Please choose one**
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

►INC4
►LPC
**►PCout (Page 172)**
►LC

**Question # 6 of 10 (Marks: 1) - Please choose one**
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

**►Accumulator** **Click here for detail**
►Address Mask
►Instruction Register
►Program Counter

**Question # 7 of 10 (Marks: 1) - Please choose one**
Computer system performance is usually measured by the ----------

**►Time to execute a program or program mix** Click here for detail
►The speed with which it executes programs
►Processor's utilization in solving the problems
►Instructions that can be carried out simultaneously

**Question # 8 of 10 (Marks: 1) - Please choose one**
Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
►Instruction Register
►Memory address register
►Memory Buffer Register
**►Registers A and C (Page 152)**

**Question # 9 of 10 (Marks: 1) - Please choose one**
---------- performs the data operations as commanded by the program instructions.

►Control
**►Data path** click here for detail
►Structural RTL
►Timing

**Question # 10 of 10 (Marks: 1) - Please choose one**
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

►Instruction Register
►**Memory address register** **Click here for detail**
►Memory Buffer Register
►Registers A and C